

AMENDMENTS TO THE CLAIMS:

Please add new claims 24-34, as shown below.

This listing of claims will replace all prior versions and listings of claims in the
Application:

Claim 1 (original): A semiconductor integrated circuit device comprising:

a first conductivity type semiconductor substrate connected to a first power supply;

a second conductivity type semiconductor layer provided on said first conductivity type semiconductor substrate or at a top surface of said first conductivity type semiconductor substrate and connected to a second power supply; and

a device forming portion provided on said second conductivity type semiconductor layer, with a decoupling capacitor formed at an interface between said first conductivity type semiconductor substrate and said second conductivity type semiconductor layer.

Claim 2 (original): The semiconductor integrated circuit device according to claim 1, wherein said second conductivity type semiconductor layer is provided on an entire top surface of said first conductivity type semiconductor substrate or at said entire top surface of said first conductivity type semiconductor substrate, and a bottom surface of said first conductivity type semiconductor substrate is connected to said first power supply.

Claim 3 (original): The semiconductor integrated circuit device according to claim 1, wherein said device forming portion has a first conductivity type well contacting said second conductivity type semiconductor layer and connected to a third power supply and another decoupling capacitor is formed at an interface between said first conductivity type well and said second conductivity type semiconductor layer.

Claim 4 (original): The semiconductor integrated circuit device according to claim 1, wherein said device forming portion has:

another second conductivity type semiconductor layer electrically connected to said second conductivity type semiconductor layer, and

a first conductivity type well provided on said another second conductivity type semiconductor layer contacted with said another second conductivity type semiconductor layer and connected to a third power supply, and

another decoupling capacitor is formed at an interface between said first conductivity type well and said another second conductivity type semiconductor layer.

Claim 5 (original): The semiconductor integrated circuit device according to claim 3, wherein said device forming portion has an active element connected to said third power supply.

Claim 6 (original): The semiconductor integrated circuit device according to claim 3, wherein a potential of said third power supply differs from potentials of said first and second power supplies.

Claim 7 (original): The semiconductor integrated circuit device according to claim 1, wherein said first conductivity type semiconductor substrate has:

a substrate body, and

a surface portion having a lower resistivity than that of said substrate body.

Claim 8 (original): The semiconductor integrated circuit device according to claim 1, wherein said second conductivity type semiconductor layer is locally provided on said first conductivity type semiconductor substrate or at the top surface of said first conductivity type semiconductor

substrate, said device forming portion is formed in that region in the top surface of said first conductivity type semiconductor substrate where said second conductivity type semiconductor layer is not provided, and said first conductivity type semiconductor substrate is connected to said first power supply via said device forming portion.

Claim 9 (original): The semiconductor integrated circuit device according to claim 8, wherein said device forming portion has a first conductivity type well and said first conductivity type semiconductor substrate is connected to said first power supply via said first conductivity type well.

Claim 10 (original): The semiconductor integrated circuit device according to claim 8, wherein said first conductivity type semiconductor substrate has:

a substrate body, and

a surface portion having a lower resistivity than that of said substrate body.

Claim 11 (original): The semiconductor integrated circuit device according to claim 10, wherein said substrate body has a resistivity of $100\ \Omega\cdot\text{cm}$ or higher.

Claim 12 (original): The semiconductor integrated circuit device according to claim 1, wherein said second conductivity type semiconductor layer is connected to said second power supply via said device forming portion.

Claim 13 (original): The semiconductor integrated circuit device according to claim 12, wherein said device forming portion has a second conductivity type well and said second conductivity type semiconductor layer is connected to said second power supply via said second conductivity type well.

Claim 14 (withdrawn): A semiconductor integrated circuit device comprising:

a first conductivity type semiconductor substrate connected to a first power supply; and
a device forming portion provided on said first conductivity type semiconductor substrate and having a second conductivity type well connected to a second power supply, with a decoupling capacitor formed at an interface between said first conductivity type semiconductor substrate and said second conductivity type well.

Claim 15 (withdrawn): The semiconductor integrated circuit device according to claim 14, wherein said first conductivity type semiconductor substrate has:

- a substrate body, and
- a surface portion having a lower resistivity than that of said substrate body.

Claim 16 (withdrawn): A semiconductor integrated circuit device comprising:

- a substrate;
- a first first conductivity type semiconductor layer connected to a first power supply provided at least a part of said substrate;
- a second conductivity type semiconductor layer provided on said first first conductivity type semiconductor layer and connected to a second power supply; and
- a device forming portion provided on said second conductivity type semiconductor layer, with a decoupling capacitor formed at an interface between said first first conductivity type semiconductor layer and said second conductivity type semiconductor layer.

Claim 17 (withdrawn): The semiconductor integrated circuit device according to claim 16, wherein said first first conductivity type semiconductor layer is provided selectively on said substrate, said device further comprises a second first conductivity type semiconductor layer, provided in that region where said first first conductivity type semiconductor layer and said

second conductivity type semiconductor layer are not provided, connected to said first first conductivity type semiconductor layer and said first power supply, and said first first conductivity type semiconductor layer is connected to said first power supply via said second first conductivity type semiconductor layer and said device forming portion.

Claim 18 (withdrawn): The semiconductor integrated circuit device according to claim 17, wherein said device forming portion has a first conductivity type well and said first first conductivity type semiconductor layer is connected to said first power supply via said second first conductivity type semiconductor layer and said first conductivity type well.

Claim 19 (withdrawn): The semiconductor integrated circuit device according to claim 17, further comprising a third first conductivity type semiconductor layer provided between said substrate and said first first conductivity type semiconductor layer and connected to said first first conductivity type semiconductor layer and said second first conductivity type semiconductor layer.

Claim 20 (withdrawn): The semiconductor integrated circuit device according to claim 16, wherein said substrate has a resistivity of 100 $\Omega \cdot \text{cm}$ or higher.

Claim 21 (withdrawn): The semiconductor integrated circuit device according to claim 16, wherein said second conductivity type semiconductor layer is connected to said second power supply via said device forming portion.

Claim 22 (withdrawn): The semiconductor integrated circuit device according to claim 21, wherein said device forming portion has a second conductivity type well and said second conductivity type semiconductor layer is connected to said second power supply via said second conductivity type well.

Claim 23 (withdrawn): The semiconductor integrated circuit device according to claim 14, wherein said device forming portion has an active element connected to third and fourth power supplies, and a potential of said third power supply differs from potentials of said first and second power supplies.

Claim 24 (new): A semiconductor integrated circuit device comprising:

a semiconductor layer;

a first region of a first conductivity type provided in said semiconductor layer, said first region being electrically connected to a first power supply; and

a second region of a second conductivity type opposite to said first conductivity type provided in contact with said first region and in said semiconductor layer, said second region being electrically connected to a second power supply, wherein a pn junction between said first region and said second region acts as a decoupling capacitor suppressing a variation of at least one of voltages supplied by said first and second power supplies.

Claim 25 (new): The semiconductor integrated circuit device according to claim 24, wherein said first and second regions spread in parallel with a main surface of said semiconductor layer.

Claim 26 (new): The semiconductor integrated circuit device according to claim 25, further comprising a circuit element formed in said main surface of said semiconductor layer, wherein said first and second regions are located below said circuit element.

Claim 27 (new): The semiconductor integrated circuit device according to claim 26, further comprising a third region of said first conductivity type provided in said main surface of said semiconductor layer and in contact with said second region, said third region being electrically connected to a third power supply, wherein said third region is a well in which said circuit

element is formed, and a pn junction between said second region and third region acts as another decoupling capacitor suppressing a variation of at least one of voltages supplied by said second and third power supplies.

Claim 28 (new): The semiconductor integrated circuit device according to claim 24, wherein said first region is a well formed in a main surface of said semiconductor layer, in which a circuit element is formed.

Claim 29 (new): The semiconductor integrated circuit device according to claim 28, wherein said second region spread in parallel with said main surface of said semiconductor.

Claim 30 (new): The semiconductor integrated circuit device according to claim 25, further comprising a body region of said first conductivity type provided below said first region, wherein said body region is lower in concentration of impurity than said first region.

Claim 31 (new): The semiconductor integrated circuit device according to claim 30, wherein said body region has resistivity of $100\Omega \cdot \text{cm}$ or higher.

Claim 32 (new): The semiconductor integrated circuit device according to claim 24, further comprising:

a first well of said first conductivity type in which a first circuit element is formed, said first region being electrically connected to said first power supply via said first well; and

a second well of said second conductivity type in which a second circuit element is formed, said second region being electrically connected to said second power supply via said second well.

Claim 33 (new): The semiconductor integrated circuit device according to claim 32, wherein said second region is located between said first region and said first well.

Claim 34 (new): The semiconductor integrated circuit device according to claim 32, wherein said first and second circuit elements are MOSFET having opposite conductivity type with each other.

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